A VME Readout System for the CALICE Electromagnetic Calorimeter

The CALICE-UK Collaboration

1. Introduction

The CALICE collaboration is studying the design of calorimetry for a future linear collider (LC) with centre-of-mass energies up to a TeV and is building prototypes of possible LC calorimeters. The prototype electromagnetic calorimeter (ECAL) is a tungsten-silicon sampling device. The hadronic calorimeter (HCAL) is a sampling calorimeter with steel as radiator, with two possible options for the active detector being considered. One is based on scintillator tiles read through photodetectors and with standard analogue or semi-digital electronic readout, called AHCAL for analogue HCAL. The second uses gas detectors with small pad sizes and digital electronic readout, called DHCAL for Digital HCAL.

2. The electromagnetic calorimeter

The ECAL prototype will be constructed from 30 layers of tungsten wrapped in carbon fiber. The active detectors will be silicon diode wafers with a pad size of $1\times1cm^2$. The very front end (VFE) electronics will provide preamplification and will be located outside of the active area, but on the same PCB as the silicon wafers. This PCB will then be connected via cables to VME readout electronics which provide digitization and readout. These are described in more detail below.

3. The VME readout system

The readout of the full prototype, where there are about 10,000 channels, will be done with six custom designed VME64 9U readout boards. These have been developed by the UK groups and were originally based on the CMS tracker readout front-end board (FED). The timing, multiplexing and calibration control for the VFE board are sent as LVDS signals by the readout board. The multiplexed analogue differential VFE channel outputs are digitised on the board using a 16-bit, 500 kHz ADC, which allows complete readout of the VFE PCB within 100 μs. The resulting ADC data are buffered in an 8 MByte on-board memory, allowing up to 2000 events to be stored before VME access is needed. This should allow an event rate above 2 kHz during a spill and the goal is to achieve an average of more than 100Hz over a run.

Each board contains ten Xilinx Virtex-II FPGAs which total around 12M gates. There are three separate designs used in the FPGAs and these are loaded using the Xilinx System ACE solution from CompactFlash cards. The boards have a high degree of flexibility as most of the front panel connector I/O is tracked directly to the FPGA pins, allowing most signals to be modified through firmware redesign. This will allow the boards to be used for reading out the HCAL prototypes; in particular, the DHCAL, which has an all digital interface, is being considered.

Two prototypes of the readout boards were produced in November, of which one is shown in fig. 1. The full system of six boards is scheduled for fabrication in summer 2004. Results from these

production boards will be presented at the conference. The two prototype boards have been used in a cosmic test bench to read out the prototype PCBs. Figure 2 shows the cosmic signal in the prototype ECAL wafers measured using these boards.

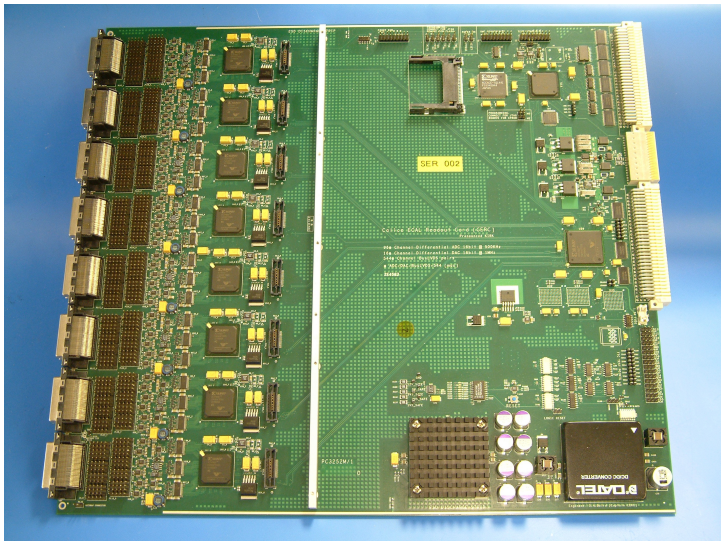

Figure 1: Prototype VME readout board.

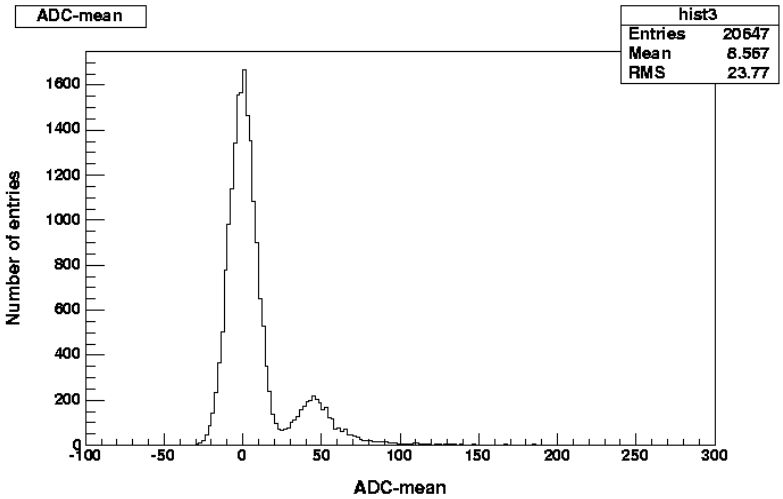

Figure 2: Pedestal and cosmic MIP signal on a prototype PCB taken with the VME prototype board.